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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/884,517	06/19/2001	Eugene A. Fitzgerald	Amber.5994A	2548

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EXAMINER
DUONG, KHANH B

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 06/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/884,517	FITZGERALD ET AL.	
	Examiner	Art Unit	
	Khanh Duong	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-12,15 and 17-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-12,15 and 17-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *16* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

This Office Action is in response to the amendment filed on March 28, 2003.

Accordingly, claims 2, 13, 14 and 16 were canceled, and claims 1 and 15 were amended.

Currently, claims 1, 3-12, 15 and 17-27 remain pending in the application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 1, 4, 6, 12, 15, 18, 20, 26 and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Lustig et al. (U.S. 5,998,807).

Re claims 1 and 15, Lustig et al. discloses a CMOS circuit (see Figs. 1-9 and corresponding description) comprising : a heterostructure including a Si substrate 1, a relaxed $Si_{1-x}Ge_x$ layer 4 on the Si substrate 1, and a strained surface layer 5 on the relaxed $Si_{1-x}Ge_x$ layer 4; and a pMOSFET (p-channel transistor) and an nMOSFET (n-channel transistor), wherein the channel of the pMOSFET and the channel of the nMOSFET are formed in the strained surface layer 5. Furthermore, since Lustig et al. discloses at

column 4, lines 1-4 the step of reducing the monocrystalline layer (positioned between the strained surface layer 5 and the Si substrate 1) to a "desired thickness" by oxidation and etching, it must be inherent that such thickness is uniform throughout the entire monocrystalline layer. Therefore, since the thickness is the same throughout the entire layer, it must also be inherent that the top surface of the monocrystalline layer is flat, smooth or planar as a result of the reducing step.

Re claims 4 and 18, Lustig et al. expressly discloses in Figures 1-9 that the heterostructure further comprises an oxide layer 2 positioned between the relaxed $Si_{1-x}Ge_x$ layer 4 and the substrate 1.

Re claims 6 and 20, Lustig et al. expressly discloses at column 3, line 60 that the strained surface layer 5 comprises silicon.

Re claims 12, 26 and 27, since the circuit as disclosed by Lustig et al. comprises a CMOS inverter (see col. 2, lines 44-48), it should be inherent that the gate drive is reduced to lower power consumption, and the p-channel transistor serves as a pull-up transistor while the n-channel transistor serves as a pull-down transistor in the circuit.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 3, 7-11, 17 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lustig et al. (U.S. 5,998,807).

Re claims 3, 7-11, 17 and 21, Lustig et al. fails to show the specific parameters regarding the surface roughness of the strained layer, the Ge content "x" in the SiGe layer, or the ratio of gate width of the pMOSFET to the gate width of the nMOSFET.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Lustig et al. by selecting the specific parameters as required by the claims, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Claims 5 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lustig et al. (U.S. 5,998,807) in view of Chu et al. (U.S. 5,906,951).

Re claims 5 and 19, Lustig et al. fails to show a SiGe graded buffer layer positioned between the relaxed $Si_{1-x}Ge_x$ layer and the Si substrate.

Chu et al. expressly teaches in Figure 1 to form a SiGe graded layer 13 positioned between the relaxed $Si_{1-x}Ge_x$ layer 14 and the Si substrate 12.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Lustig et al. with the teaching of Chu et al., since Chu et al. states at column 1, lines 32-43 that such modification would provide a buffer layer with low dislocation densities.

Claims 22-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lustig et al. (U.S. 5,998,807) in view of Kant (U.S. 6,316,301).

Re claims 22-25, Lustig et al. fails to specify what types of devices could be formed using a CMOS circuit.

Kant teaches that CMOS circuits are used to form an inverter (see Fig. 1; col. 1, lines 37-40) and a number of suitable logic gates such as NOR gates, XOR gates and NAND gates (see Fig. 4; col. 4, lines 20-22).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the CMOS circuit of Lustig et al. to form the devices as suggested by Kant because of the desirability to perform a variety of functions.

Response to Arguments

Applicant's arguments filed March 28, 2003 have been fully considered but they are not persuasive.

Applicants persistently argues that Lustig et al. does not disclose a planarized surface positioned between the strained surface layer and the Si substrate. The Examiner disagrees because Lustig et al. clearly discloses, as previously stated above, the step of reducing a monocrystalline layer, which is positioned between the strained surface layer 5 and the Si substrate 1, to a "desired thickness" or uniform thickness, which ultimately

equates to a flattened, smoothed or planarized top surface for the monocrystalline layer (see Lustig et al., column 4, lines 1-4).

Applicant also argues that Chu et al. and Kant fail to cure the deficiences of Lustig et al.. Since Lustig et al. clearly discloses a planarized surface positioned between the strained surface layer and the Si substrate as described above, argument regarding Chu et al. and Kant is moot. Furthermore, in response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Duong whose telephone number is (703) 305-1784. The examiner can normally be reached on Monday - Friday (9:00 AM - 6:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian, can be reached on (703) 308-4905. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3431 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

KBD
June 12, 2003

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800